UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,589	08/24/2001	Mahito Shinohara	35.C15697	3628

5514 7590 06/02/2005

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,589	SHINOHARA, MAHITO	
	Examiner	Art Unit	
	Justin P. Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6,8,10 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,8,10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 13 December 2004 have been fully considered but they are not persuasive; however, the Examiner accepts Applicant's amendments to the specification and drawings.

2. Applicant argues, "the signal Rx is supplied independently of a signal level of an output line ("data out"), and the control electrode of the reset transistor is not connected to the output line."

3. The Examiner disagrees with Applicant's position. The claim language does not specifically require that a control electrode of the reset transistor be supplied with a control signal, which controls an on/off of the reset transistor and wherein the control signal is directly connected to the pixel output line. Rather, the claim language is written broadly enough such that it only requires that the reset transistor be turned on and off, via the control electrode area, in accordance to a pixel signal output and that the control electrode area is connected to the output line.

4. In regards to Kim et al., figure 5 clearly teaches the interpretation above. Initially, it is important to note that since the resent transistor is connected to the output line, the control electrode area of the reset transistor is also connected to the output line. Furthermore, the "data out" line outputs the pixel signal level of the photodiodes 401 and 402 when the selection transistor M4 is turned on at time period C1 and the "data out" line is reset to VDD, via reset transistor M1, at time period C2. Kim et al. clearly discloses wherein the reset transistor (M1) is

controlled to be turned on and off in accordance with the pixel signal level of said output line (data out) because it is not until the actual pixel signal level of the photodiodes is present on the output line (data out) that the reset transistor (M1) is turned on.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 3, 6, 8, 10, and 12** are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al.

7. For **Claim 1**, Kim et al. disclose, as shown in figures 1, 4, and 5 and as stated in columns 4 (lines 60 – 67) and 5 (lines 1 – 24), a solid-state image pickup apparatus (400) comprising:

a pixel (400) including a photoelectric conversion unit (401 and 402), a read transistor (M3) for reading a signal from said photoelectric conversion unit (401 and 402), and a reset transistor (M1) for resetting an input portion of said read transistor (M3; When the reset transistor M1 is turned on, vdd flows through the reset transistor M1 and onto the gate of the read transistor M3, thereby also turning on the read transistor M3, wherein vdd also flows through an source input portion of the read transistor M3); and

an output line (data-out) to which the signal from the read transistor (M3) is read out (by means of selecting transistor M4), said output line (data-out) being connected to a control

electrode area (via the reset transistor M1) of the reset transistor (In other words, since the resent transistor is connected to the output line, the control electrode area of the reset transistor is also connected to the output line.)

wherein the reset transistor (M1) is controlled to be turned on and off by changes in voltage at said control electrode area in accordance with a signal level of said output line (data-out; see explanation below).

The claim language is written broad enough such that it only requires that the reset transistor be turned on and off, via the control electrode area, in accordance to a pixel signal output and that the control electrode area is connected to the output line.

In regards to Kim et al., figure 5 clearly teaches the interpretation above. Initially, it is important to note that since the resent transistor is connected to the output line, the control electrode area of the reset transistor is also connected to the output line. Furthermore, the "data out" line outputs the pixel signal level of the photodiodes 401 and 402 when the selection transistor M4 is turned on at time period C1 and the "data out" line is reset to VDD, via reset transistor M1, at time period C2. Kim et al. clearly discloses wherein the reset transistor (M1) is controlled to be turned on and off in accordance with the pixel signal level of said output line (data out) because it is not until the actual pixel signal level of the photodiodes is present on the output line (data out) that the reset transistor (M1) is turned on.

8. As for **Claim 3**, Kim et al. disclose, as shown in figure 4, a control transistor (select transistor M4) connected to said output line (data-out) to control the signal level of said output line (select transistor M4 turns the control line on or off).

9. As for **Claim 6**, Kim et al. disclose, as stated in column 2 (lines 64 – 67), wherein the read transistor and reset transistor are MOS transistors.

10. As for **Claim 8**, Kim et al. disclose, as shown in figures 4 and 5, a transfer switch (M43) between the photoelectric conversion unit (401) and the read transistor (M3), wherein signal charges accumulated in the photoelectric conversion unit are transferred to the input portion of the read transistor through said transfer switch (At time period F1).

11. As for **Claim 10**, Kim et al. disclose, as shown in figures 4 and 5, wherein a plurality of transfer switches (M43 and M44) are connected to the input portion of the read transistor (The transfer switches M43 and M44 are connected to the gate of read transistor M3 and to the source of read transistor M3, by means of reset transistor M1), and signal charges are independently transferred from a plurality of photoelectric conversion units by said transfer switches (In independent time periods F1 and F2; see figure 5).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al.

14. As for **Claim 12**, Kim et al. do not disclose an image pickup system comprising said solid-state image pickup apparatus; an optical system adapted to form an image of light onto said solid-state image pickup apparatus; and a signal processing circuit adapted to process an output

signal from said solid-state image pickup apparatus. **Official Notice** is taken that both the concepts and the advantages of providing an image pickup system comprised of an optical system and a signal processing circuit are well known and expected in the art. It would have be obvious to one with ordinary skill in the art to have provided an image pickup system comprised of an optical system and a signal processing circuit as a means to generate a focused, high resolution, low noise digital image.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:00 PM and on alternating Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 571.272.7308. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
May 30, 2005

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2500